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(54) Title of the invention Clock driver circuit
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Specification

Title of the invention

Clock driver circuit

Claims

A clock driver circuit for obtaining complementary clock signals for clocking signals, characterized by the fact that it is provided with:
a first logic circuit having a first input terminal connected to a clock input terminal and an output terminal connected to a first clock output terminal; and
an inversion circuit having an input terminal connected to the clock input terminal;
a second logic circuit having a first input terminal connected to the output terminal of the inversion circuit; and
an output terminal connected to a second clock output terminal, a first delay time selection circuit having an input terminal and an output terminal connected to the output terminal of the first logic circuit and the second input terminal of the second logic circuit, respectively, and having:
at least one control terminal for selecting delay time, and
a second delay time selection circuit having an input terminal and an output terminal connected to the output terminal of the second logic circuit and the second input terminal of the first logic circuit, respectively, and having:
at least one control terminal for selecting the delay time.

Detailed explanation of the invention

[Scope of the invention]

The present invention relates to a clock driver circuit, and relates in particular to a clock driver circuit for producing clock pulses that do not overlap with one another in a synchronous sequential circuit or a DAC circuit.

[Prior art technology]

Prior art clock driver circuits use NOR logic circuits, an inverter circuit, and delay circuits to generate complementary clocks.

Fig.7 is a block diagram of an exemplary prior art clock driver circuit.

As shown in Fig.7, the clock driver circuit has two-input NOR logic circuits 4 and 7, an inverter 10, and delay circuits 23 and 24 for delaying the output clocks of the logic circuits 4 and 7. Clocks from an input terminal 1 are obtained from a first output terminal 2 as complementary clocks, with the phase being inverted and from a second output terminal 3 as delayed clocks. In this instance, the delay times of the delay circuits 23 and 24 are sufficiently larger than the delay time of a gate step.

Fig.8 is a signal waveform chart to explain the operation of the clock driver circuit shown in Fig.7.

As shown in Fig.8, when the clock input signal is low or the input terminal 1 is low, the inverter 10, two-input NOR 4, and delay circuit 23 have high output and the two-input circuits NOR 7 and delay circuit 24 have low output. When the input signal is changed from low to high, the inverter 10 has low output and the output of the two-input NOR 4 or the first output terminal 2 is changed to low. The low output is delayed by the delay circuit 23 before being applied to the two-input circuit NOR 7. Then, the output of the two-input NOR 7 or the second output terminal 3 is changed from low to high. Then, when the input signal is changed from high to low, the inverter 10 has high output and the output of the two-input NOR 7 or the second output terminal 3 is changed from high to low. This low output is delayed by the delay circuit 24 before it is applied to the two-input NOR 4. Then, the output of the two-input NOR 4 or the first output terminal 2 is changed from

low to high. In this way, the first output terminal 2 and second output terminal 3 can produce complementary clocks, the high outputs of which do not overlap by the delay time determined by the delay circuit 23 or 24.

[Problems overcome by the invention]

The prior art clock driver circuit described above delays the inversion of complementary clocks by a fixed time determined by the delay circuit. It is difficult to select the clock once it is mounted in a semiconductor integrated circuit.

The purpose of the present invention is to provide a clock driver circuit producing complementary clocks with a variable delay time.

[Problem resolution means]

The clock driver circuit of the present invention, in a clock driver circuit which obtains complementary clock signals from among clock signals, is composed of a first logic circuit having a first input terminal connected to a clock input terminal and an output terminal connected to a first clock output terminal, an inversion circuit having an input terminal connected to the clock input terminal, a second logic circuit having a first input terminal connected to the output terminal of the inversion circuit and an output terminal connected to a second clock output terminal, a first delay time selection circuit having an input terminal and an output terminal connected to the output terminal of the first logic circuit and the second input terminal of the second logic circuit, respectively, and is provided with at least one control terminal for selecting delay time, and a second delay time selection circuit having an input terminal and an output terminal connected to the output terminal of the second logic circuit and the second input terminal of the first logic circuit, respectively, and having at least one control terminal for selecting delay time

[Embodiments]

Embodiments of the present invention are described hereafter, with reference to the drawings.

Fig.1 is a block diagram of Embodiment 1 of the block driver circuit of the present invention.

As shown in Fig.1, this embodiment comprises two-input NOR circuits 4 and 7, an inverter 10, and delay time selection circuits 5 and 8 having control terminals 6 and 9, respectively. The clock input from an input terminal 1 is output as a complementary clock from a first output terminal 2 and a second output terminal 3. Here, it is assumed that selected delay times of the delay time selection circuits 5 and 8 are sufficiently larger than the delay time of one gate step as in the prior art described above.

Fig.2 is a signal waveform chart to explain the operation of the clock driver circuit shown in Fig.1.

As shown in Fig.2, when the clock input signal is low or the input terminal 1 is low, the inverter 10, first two-input NOR 4, and first delay time selection circuit 5 have high output and the second two-input NOR 7 and second delay time selection circuit 8 have low output. Then, when the input signal is changed to high, the inverter 10 has low output and the output of the two-input NOR 4 or the first output terminal 2 is changed to low. This low output is delayed by the delay time selection circuit 5 before it is applied to the two-input NOR 7. Then, the output of the two-input NOR 7 or the second output terminal 3 is changed from low to high. When the input signal is changed to low, the inverter 10 has high output and the output of the two-input NOR 7 or the second output terminal 3 is changed to low. The low output is delayed by the delay time selection circuit 8 before being applied to the two-input NOR 4. Then, the output of the two-input NOR 4 or the first output terminal 2 is changed from low to high.

In this way, the first output terminal 2 and second output terminal 3 is able to produce a complementary clock the high output of which is not overlap by the delayed time determined by the delay time selection circuit 5 or 8 in relation to an input clock.
Fig.3 is an illustration to show the structure of an embodiment of the delay time selection circuit shown in Fig.1.

As shown in Fig.3, the delay time selection circuit 5 or 8 comprises a first delay circuit 13 connected to an input terminal 11, a first switch 16 connected to the delay circuit 13 and a circuit for short-circuiting the delay circuit 13, a second delay circuit 14 connected to the switch 16, a second switch 17 connected to the delay circuit 14 and a circuit for short-circuiting the delay circuit 14, a third delay circuit 15 connected between the switch 17 and an output terminal 12, and a decoder circuit 18 for controlling the switches 16 and 17 based on control signals from control terminals 9. Particularly, control signals 9 are

input to the decoder circuit 18 and decoded decoder outputs 19 and 20 are used to control the switches 16 and 17.

Fig.4 is a signal waveform chart to explain the operation of the delay time selection circuit shown in Fig.3.

Fig.4 shows the signal waveform of three clock outputs (a) to (c) at the output terminal 12 for an input clock at the input terminal 11.

For example, as shown in Fig.4, when both switches 16 and 17 close the lower paths, the input signal at the input terminal 11 pass through only the delay circuit 15 so that it is delayed as shown as a clock output (a) before it is output at the output terminal 12. Similarly, when the switches 16 and 17 are controlled by the decoder circuit 18 based on input values of the control signals 9, the output can be delayed as shown as a clock output (b) or (c) before it is output at the output terminal 12.

Fig.5 is a block diagram of Embodiment 2 of the clock driver circuit of the present invention.

As shown in Fig.5, this embodiment is the same as Embodiment 1 except that a two-input NAND 21 is used as a first logic circuit and a two-input NAND 22 is used as a second logic circuit.

Fig.6 is a signal waveform chart to explain the operation of the clock driver circuit shown in Fig.5.

As shown in Fig.6, when the input signal from the input terminal 1 is low, the two-input NAND 21 and inverter 10 have high output and the delay time selection circuit 5 also has high output. Thus, the two-input NAND 22 has two high input and, therefore, produces low output. Then, when the input signal is changed to high, the inverter 10 has low output and the output of the two-input NAND 22 or the second output terminal 3 is changed to high. This low output is delayed by the delay time selection circuit 8 before being applied to the two-input NAND 21. Therefore, the output of the two-input NAND 21 or the first output terminal 2 is changed from high to low. Then, when the input signal is changed from high to low, the inverter 10 has high output and the output of the two-input NAND 21 or the first output terminal 2 is changed from low to high. This high

output is delayed by the delay time selection circuit 5 before it is applied to the two-input NAND 22. Then, the output of the two-input NAND 22 or the second output terminal 3 is changed from high to low.

In this way, the first output terminal 2 and second output terminal 3 can produce complementary clocks the low output of which are not overlapped by the delay time determined by the delay time selection circuit 5 or 8 in relation to input clocks.

[Efficacy of the invention]

As described above, the clock driver circuit of the present invention comprises two delay time selection circuits for changing delay time using respective control terminals so that the inversions of complementary signals are delayed in relation to the clock input by an arbitrarily selected time.

[Brief explanation of the drawings]

Fig.1 is a block diagram of Embodiment 1 of the clock driver circuit of the present invention.

Fig.2 is a signal waveform chart to explain the operation of the clock driver circuit shown in Fig.1.

Fig.3 is an illustration to show the structure of an embodiment of the delay time selection circuit shown in Fig.1.

Fig.4 is a signal waveform chart to explain the operation of the delay time selection circuit shown in Fig.3.

Fig.5 is a block diagram of Embodiment 2 of the clock driver circuit of the present invention.

Fig.6 is a signal waveform chart to explain the operation of the clock driver circuit shown in Fig.5.

Fig.7 is a diagram to show a prior art clock driver circuit.

Fig.8 is a signal waveform chart to explain the operation of the clock driver circuit shown in Fig.7.

1...input terminal, 2...first output terminal, 3...second output terminal, 4,7...NOR logic circuit, 5,8...delay time selection circuit, 6,9...control circuit, 10...inversion circuit (inverter), 11...input terminal, 12...output terminal, 13 to 15...delay circuit, 16,17...switch, 18...decoder circuit, 19.20...decoder output, 21,22...NAND logic circuit.

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[Fig.1]

1 input terminal
2 first output terminal
3 second output terminal
4 logic circuit
5 delay time selection circuit
6 control terminal

[Fig.2]

Clock input
NOR 4 output
Delay time selection circuit 5 output
Inverter 10 output
NOR 7 output
Delay time selection circuit 8 output

[Fig.3]

13 delay circuit
16 switch
18 decoder circuit

[Fig.4]

Clock input
Clock output (a)
Clock output (b)
Clock output (c)

[Fig.5]

[Fig.6]

Clock input
NAND 21 output
Delay time selection circuit 5 output
Inverter 10 output
NAND 22 output
Delay time selection circuit 8 output

[Fig.7]

[Fig.8]
Clock input
NOR 4 output
Delay circuit 23 output
Inverter 10 output
NOR 7 output
Delay circuit 24 output